REMARKS

Reconsideration of the application is requested.

Claims 1-8 remain in the application. Claims 1 and 3-8 have been amended. Claim 2 has been canceled.

In "Claim Objections" on page 2 of the above-identified Office Action, the Examiner objected to claims 3-7 because of alleged informalities. The Examiner's suggested corrections have been made although it is believed that there is no informality in referring, for example, to "a capacitance" when the antecedent is "a frequency-determining capacitance" if no other capacitance is mentioned. For consistency in view of the Examiner's objections, the term "oscillator" where used alone has been changed to "voltage controlled oscillator" in claims 1 and 8.

In "Claim Rejections - 35 USC § 103", item 3 on pages 3-4 of the above-identified Office Action, claims 1-8 have been rejected as being obvious over U.S. Patent No. 4,074,209 to Lysobey in view of International Publication No. WO 89/06456 to Davis under 35 U.S.C. § 103(a).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the

instant application. Support for the changes is found in original claim 2 and on page 6, first paragraph of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a phase locked loop for open loop mode, comprising:

> a voltage controlled oscillator having a first tuning input for a tuning voltage and a signal output for an output signal of tunable frequency;
>
> said voltage controlled oscillator having a frequency-determining capacitance controlled using a second tuning input;
>
> a frequency divider having an adjustable division ratio for the purpose of channel adjustment for the phase locked loop, having an input coupled to said signal output of said voltage controlled oscillator, having an output carrying a frequency-divided output signal and coupled to said first tuning input of said voltage controlled oscillator in a control loop, and having a control input for stipulating the division ratio;
>
> a loop filter having a memory effect;
>
> a phase detector having a first input connected to said output of said frequency divider, a second input connected to a reference frequency source, and an output connected via said loop filter to said first tuning input of said voltage controlled oscillator; and
>
> a frequency stipulation unit for programming the frequency of the output signal of tunable frequency connected, firstly, to said control input of said frequency divider for transmitting a frequency word and, secondly, to said second tuning input of said voltage

controlled oscillator for transmitting the frequency word such that a change in the tuning voltage upon a change in the frequency word disappears or is as small as possible in order to avoid any frequency drift in an open loop mode of the phase locked loop;

said voltage controlled oscillator having resonant frequency preselection to compensate for the memory effect of said loop filter.

It is an object of the present invention, as recited in amended claim 1, to avoid problems with capacitor soakage within a loop filter of a phase locked loop or PLL circuit. Capacitor soakage leads to an undesired memory effect within the loop filter. In an open-loop mode of the PLL, the memory effect will detune the output frequency of the voltage controlled oscillator or VCO because the capacitor voltage of the filter attempts to return to its previous value.

In order to overcome this problem, the present invention proposes keeping the filter voltage virtually constant. This, of course, also means providing a constant tuning voltage. According to the present invention, a constant tuning voltage even with a different frequency channel is achieved by providing additional tuning within the oscillator. This additional tuning, referred to in claim 1 as "frequency-determining capacitance controlled using a second tuning input" is controlled by a frequency stipulation unit. This frequency stipulation unit is used for

programming the frequency of the output signal by programming the divider ratio of the frequency divider within the loop. The control of the additional loop filter capacitance is performed in such a way that, at the input of the VCO, the voltage, namely the tuning voltage, remains virtually the same. By doing this, the loop filter which is connected to a first tuning input of the oscillator also has a virtually constant filter voltage even when a channel of the PLL is changed.

This has advantages when applied in systems which are implemented by using frequency hopping and time division duplex or TDD, in such a way that they work with time slots. The frequency is changed significantly between the time slots. These systems are applied within many mobile communication standards such as the global system for mobile communication or GSM, which still dominates certain telecommunication markets in the field of cellular phones.

After carefully considering the arguments presented by the Examiner in the final Office action, Applicants believe that there is a substantial difference between the present invention as recited in amended claim 1 and the teaching of Lysobey and Davis.

The Lysobey reference discloses a PLL having a wide range frequency modulation and, at the same time, a narrow loop bandwidth. This is achieved by implementing a so-called Tow-Point modulation. This means that a modulation signal V_M is fed both into a phase comparator 15 and into the VCO 19, as is seen, for example, in Figs. 1 and 3 of Lysobey. By doing this, the modulation signal is fed into the PLL at a coupling node having high-pass characteristics and at another coupling node having low-pass characteristics. However, according to the teachings of Lysobey, a significant change of the sensitivity of the VCO has been observed over the desired wide range of frequency modulation which is possible with the Two-Point modulation principle taught in Lysobey. This problem of a variation of the sensitivity of the VCO is undesired in Lysobey, because it leads to a variation of the output signal of the PLL as a response of the modulation signal. Therefore, in Fig. 3 and the accompanying description, Lysobey teaches avoidance of the undesired effect of a variation of the sensitivity of the VCO which occurs with a Two-Point modulation over a frequency wide range in combination with a small loop bandwidth.

According to Fig. 3 of Lysobey, the modulation signal is fed via a resistor R2 to varactors as well as via a modulator 11 into a phase comparator 15. In addition to this, in order to

compensate for the modulating voltage within the VCO directly fed into it, the frequency selection signal fed into an input terminal 32 is also fed, via a D/A converter 33, into the modulating varactors VC1 and VC2 via the resistor R1 and inductors L1, L2. As is taught by the wording of Lysobey, the binary signal, namely the frequency selection signal, is also applied to supply the signal which biases the VCO modulator in a direction to correct for the change in the VCO sensitivity, referred to as K, as is discussed in column 5, lines 22 to 25 of Lysobey.

Therefore, there can be no doubt about the fact that Lysobey teaches keeping the *sensitivity* of the VCO constant over a wide modulation frequency range.

The present invention, however, solves a different problem. With the present invention, as explained above in more detail, a frequency drift in an open-loop mode of the phase locked loop as a response to a varying tuning voltage due to channel switching is compensated for. According to the present invention, the tuning voltage of the loop is kept constant independently of a change of the frequency word fed into the PLL. In contrast thereto, Lysobey does not teach keeping the tuning voltage constant, but instead teaches providing a constant sensitivity K of the oscillator of the

loop. Applicants believe that these are two completely different approaches.

The wording referred to by the Examiner in Item 4 of the final Office action, Response to Arguments, refers to column 3, lines 30 to 35 of Lysobey. This portion of the reference refers to Figs. 1 and 2 of Lysobey, not to Fig. 3 thereof. The goal of making the system output signal independent of the loop transfer function or response is achieved by the circuit of Fig. 2, as described in column 3, lines 37 to 40. This does not imply more features than the Two-Point modulation discussed above. By implementing the Two-Point modulation as shown in Fig. 2 of Lysobey, one modulation point having high-pass characteristics and one modulation point having low-pass characteristics are provided. Doing this achieves the goal of having a wide range frequency modulation even when, at the same time, the loop bandwidth is narrow. Nothing else is taught in the description of Fig. 2 of Lysobey.

Fig. 3 and the accompanying description of Lysobey, however, deal with an additional problem which occurs when applying the Two-Point modulation. This additional problem is an undesired variation of K, namely the sensitivity of the oscillator, over the wide modulation frequency range. In

order to compensate for the variation of the sensitivity, the frequency selection signal is fed into the VCO core. However, it has to be emphasized that according to the disclosure of Lysobey there is no teaching of how to keep the tuning voltage of the VCO constant as in the present invention. Lysobey is completely silent on this aspect. Both in Lysobey and with the present invention, an additional compensation signal is fed into the VCO, but for a different purpose and to achieve a different object.

Therefore, it is believed that the circuit recited in amended claim 1 of the instant application is novel and non-obvious over Lysobey.

Davis does not teach the features missing from Lysobey. Davis is also completely silent on the aspect of avoiding problems with capacitors soakage. In addition to this, Davis does not teach providing a way to ensure that the tuning voltage remains constant even if the frequency range of the PLL is switched to a different range by a channel frequency programming step. Instead, Davis provides a way to provide a core tuning, which tuning is then further modified by the normal operation of the phase-locked loop.

Therefore, neither of the references applied by the Examiner

in the Office action deals with the problem of providing a phase-locked loop which is able to be applied in full duplex communication systems and provides a reduction or compensation of the memory effect of filter capacitors.

In addition thereto, Lysobey does not explicitly teach any of the features of amended claim 1, namely the provision of a reference frequency source connected to a second input of the phase detector. Instead of this, the modulation signal V_M is connected to the phase comparator 15 of Fig. 3 of Lysobey, as described in column 4, lines 48-52 of Lysobey.

Clearly, neither Lysobey nor Davis, whether taken alone or in any combination, show or suggest the features recited in claim 1 of the instant application. Claim 1 is, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a

telephone call so that, if possible, patentable language can be worked out.

If an extension of time is required, petition for extension is herewith made. Any extension fee associated therewith should be charged to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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